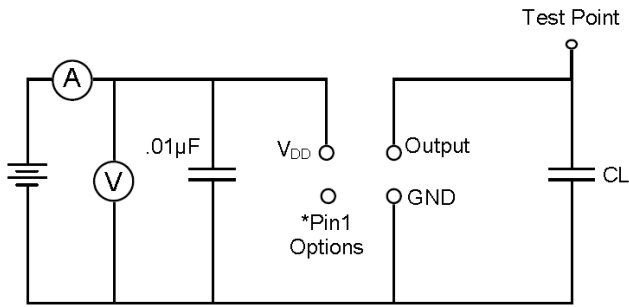
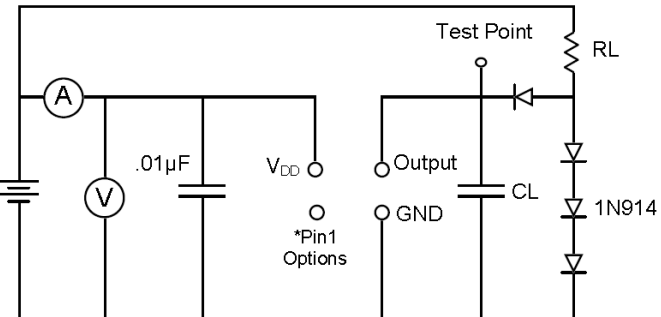
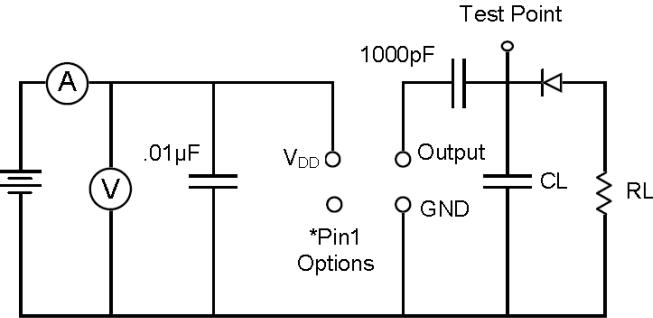
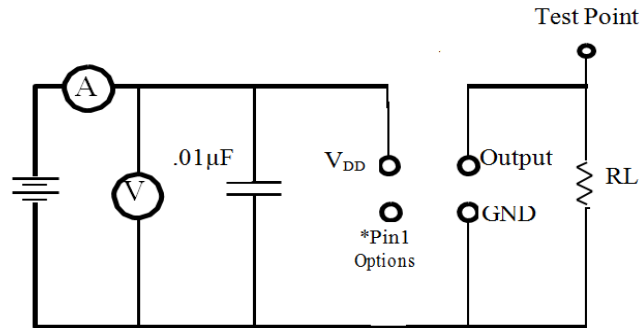


<p style="text-align: center;">CMOS</p>	 <p>The diagram shows a test circuit for a CMOS load. It includes a DC power source, an ammeter (A), a voltmeter (V), and a .01μF capacitor connected to the V_{DD} pin. The output pin is connected to a load capacitor (CL) and a test point. The test point is also connected to a resistor (RL) and a diode (1N914) to ground. The GND pin is connected to ground.</p> <div style="border: 1px solid black; padding: 5px; width: fit-content;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div> <ul style="list-style-type: none"> • CL = 15pF
<p style="text-align: center;">TTL</p>	 <p>The diagram shows a test circuit for a TTL load. It includes a DC power source, an ammeter (A), a voltmeter (V), and a .01μF capacitor connected to the V_{DD} pin. The output pin is connected to a load resistor (RL), a diode (1N914) to ground, and a test point. The test point is also connected to a load capacitor (CL). The GND pin is connected to ground.</p> <div style="border: 1px solid black; padding: 5px; width: fit-content;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div> <ul style="list-style-type: none"> • RL = 2.0kΩ (2TTL) / RL = 820Ω (2TTL) • RL = 390Ω (2TTL) / CL = 15pF
<p style="text-align: center;">Clipped Sine Wave</p>	 <p>The diagram shows a test circuit for a Clipped Sine Wave load. It includes a DC power source, an ammeter (A), a voltmeter (V), and a .01μF capacitor connected to the V_{DD} pin. The output pin is connected to a load resistor (RL), a load capacitor (CL), and a test point. The test point is also connected to a diode (1N914) to ground. The GND pin is connected to ground.</p> <div style="border: 1px solid black; padding: 5px; width: fit-content;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div> <ul style="list-style-type: none"> • RL = 10kΩ • CL = 10pF

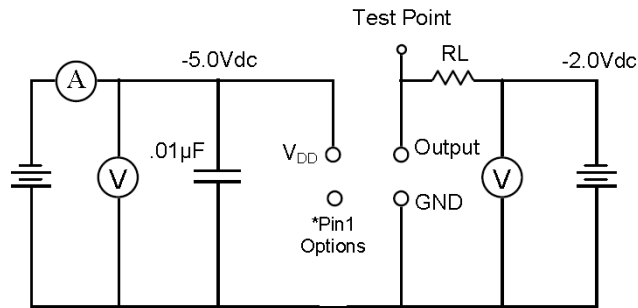
Sine Wave



$RL = 50 \Omega$

*Pin 1 Options: a. NC
b. Tri-State
c. VC

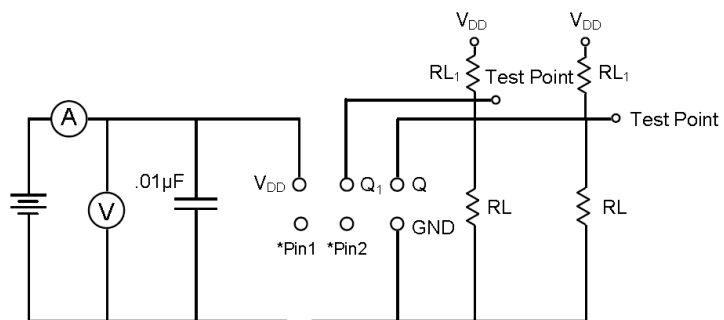
ECL



$RL = 50 \Omega$

*Pin 1 Options: a. Complementary Output
b. NC
c. Tri-State
d. VC

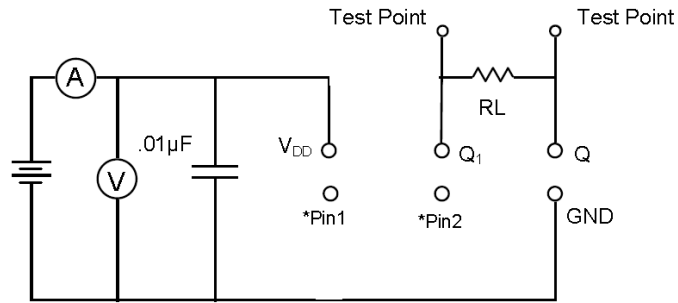
PECL



*Pin Option		
	OSC	VCXO
Pin 1	Tri-State	V _C
Pin 2	NC	Tri-State

- $RL = 82 \Omega$
- $RL1 = 124 \Omega$
- Q = Output
- Q₁ = Complementary Output

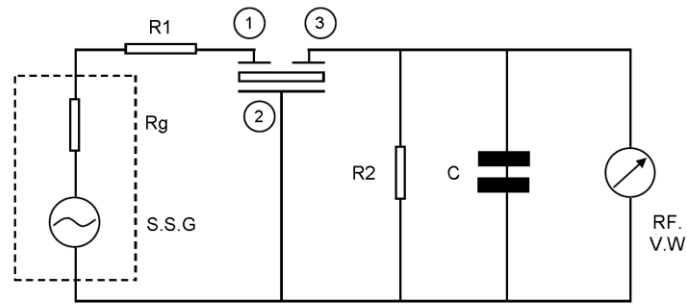
LVDS



*Pin Option		
	OSC	VCXO
Pin 1	Tri-State	V _C
Pin 2	NC	Tri-State

- RL = 100Ω
- Q = Output
- Q₁ = Complementary Output

Ceramic Filter



$R_g + R_1 = R_2 = 330\Omega$
 Impedance
 $C = 10\text{pF}$
 (Including stray Capacitance and input capacitance of Rf Voltmeter)